IN THE CLAIMS:

1-19. (Canceled)

20. (Original) A method of making an electrostatic discharge semiconductor device on a semiconductor substrate having a first conductivity type and a first doping concentration, comprising:

implanting into the substrate first, second, and third well regions having second conductivity types that are opposite in polarity to said first conductivity type;

implanting a fourth well region of the first conductivity type adjacent to said substrate and adjacent to said first well region; and

forming an insulated terminal across said second and said third well regions.

21. (Original) The method of claim 20, further comprising implanting a fifth well region into said substrate having the first conductivity type and a second doping concentration.

22. (Original) The method of claim 20, wherein implanting said fourth well comprises doping the fourth well region with a second doping concentration that is greater than the first doping concentration.

23. (Original) The method of claim 20, further comprising forming an insulated terminal above said first well region.

24. (Original) The method of claim 20, wherein said fourth well region comprises a halo region adjacent to said first well region that reduces a breakdown voltage between the first well region to the substrate.

25. (Original) The method of claim 20, wherein the fourth well region comprises forming a lightly doped drain adjacent to said first well region that reduces a breakdown voltage between said first well region to said substrate.

26. (Original) The method of claim 20, wherein said fourth well region is adjacent to said second well region that reduces a breakdown voltage between said first well region to said substrate.

27. (New) A method of making an electrostatic discharge semiconductor device, comprising the steps of:

implanting, into a substrate having a first concentration of a first conductivity type, a first region, a second region, and a third region, each of said first region, said second region, and said third region having a second conductivity type that is opposite in polarity to said first conductivity type, wherein said first region is separated from said second region and said third region by an isolation region;

implanting a fourth region of said first conductivity type adjacent to said substrate and adjacent to said first region;

implanting a fifth region of said first conductivity type and a second doping concentration into said substrate, said fifth region being separated from said first, said second, said third and said fourth regions by an isolation region;

forming an insulated terminal across said second and said third well regions;

electrically connecting said first and said second regions to an input pad of said semiconductor device; and

electrically connecting said insulated terminal, said third region and said fifth region to each other.

28. (New) The method of claim 27, wherein said fourth region comprises a halo region adjacent to said first region that reduces a breakdown voltage between said first region and said substrate.

29. (New) The method of claim 27, wherein said fourth region comprises forming a lightly doped drain adjacent to said first region that reduces a breakdown voltage between said first region and said substrate.

30. (New) The method of claim 27, wherein said fourth region is adjacent to said second region and reduces a breakdown voltage between said first region and said substrate.